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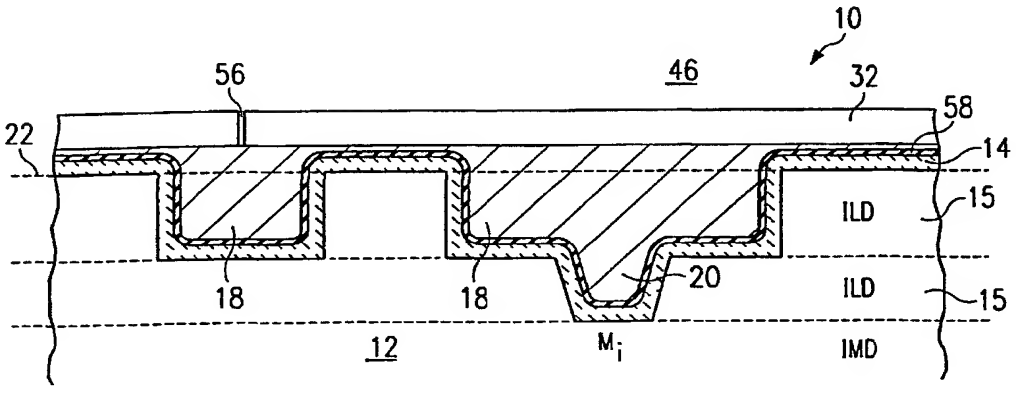

(57) Abstract: A method and apparatus for electroplating material, such as copper, into substrate formations is disclosed that substantially suppresses the electroplating of the material on the field of the substrate along the substrate surface plane. A current voltage source, applies current between a copper anode and the backside of the substrate wafer to support electroplating of material on the frontside of the substrate. Current flows through the substrate wafer to the frontside surface of the substrate wafer acting as a cathode of an electroplating circuit to provide charged copper through an electrolyte bath to electroplate the copper on the substrate. A membrane with the time modulation, conformed against the substrate surface plane, either continuously or intermittently suppresses electroplating of copper along the field regions of the substrate, resulting in a globally planarized surface without the use of chemical-mechanical polishing.

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METHOD ANS APPARATUS FOR ELECTROPLATING DEPRESSIONS OF A SUBSTRATE SIMULTANEOUSLY PREVENTING PLATING ON THE SUBSTRATE SURFACE USING A MEMBRANE COVER

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of electronic devices and semiconductor integrated circuits, and more particularly to a method and apparatus for electroplating of a material layer for fabrication of a microelectronic device such as a semiconductor integrated circuit chip interconnect metallization structure.

BACKGROUND OF THE INVENTION

The speed and reliability performance of the leading-edge semiconductor chips, particularly the logic chips such as microprocessors, that are fabricated using the 0.25 μm technology nodes and beyond is usually limited by on-chip interconnects. For instance, the maximum clock frequencies of the state-of-the-art microprocessor chips may be limited by the on-chip interconnect signal cross-talk and "RC" propagation delays due to parasitic elements of the interconnect structure, such as parasitic resistive, capacitive, and inductive elements of the interconnect metallization and inter-metal dielectric (IMD) structure. To reduce these parasitic elements and their undesirable performance degradation effects, industry has turned to

alternative materials for forming multi-level interconnects.

The primary approach pursued by the semiconductor industry is to replace conventional interconnect metallization materials, such as aluminum, aluminum alloys and tungsten, with copper due to its higher electrical conductivity (copper bulk resistivity of $\leq$ 1.8 $\mu\Omega$·cm vs. aluminum resistivity of ~ 2.7 $\mu\Omega$·cm). Another complementary approach is to replace the conventional silicon oxide inter-level dielectric (ILD) and inter-metal dielectric (IMD) layers with a suitable reduced permittivity or low-k dielectric material. These low-k dielectric materials generally complicate interconnect process integration due to their inferior thermal stability as well as their inferior electrical, mechanical and thermal conductivity properties compared to silicon dioxide.

Although, over the next several years, copper is expected to become the metallization material of choice for use in most high-performance silicon integrated circuit applications, a number of difficulties exist with the deposition and integration of copper. For instance, due to the technological and manufacturing difficulties associated with dry etching of copper, the primary approach for copper metallization is to form inlaid metal lines and plugs of a substrate formation based on either the single or the dual damascene techniques, which eliminate the need for metal etch processes, for instance by using chemical-mechanical polishing or CMP process.

Typically, the dual damascene technique involves two microlithography patterning steps and two anisotropic dielectric etching steps to form interconnect via holes, for supporting inter-level metal plug connections, and to

form the dielectric trench pattern, for supporting inlaid copper metallization lines. A thin diffusion barrier layer is generally deposited before copper deposition to prevent copper diffusion into the ILD/IMD layers, which would degrade their electrical properties and poison the silicon devices during the remaining device fabrication steps and during the actual chip operation. A copper layer is then generally deposited as a blanket layer covering and filling not only the line trenches and via holes, but also the remainder of the substrate, including the substrate field regions. Chemical-mechanical polishing (CMP) is then used to selectively remove excess copper and barrier from the substrate field regions, polishing back the copper metal to expose the underlying substrate (e.g., field dielectric regions) and to establish the patterned inlaid metal lines and plugs. This process sequence is generally repeated for each interconnect level until the multi-level interconnect fabrication process flow is complete.

Conventional damascene techniques for formation of inlaid metallization structures have a number of disadvantages due to fabrication process complexities and costs. One significant disadvantage is the need for chemical-mechanical polishing (CMP) which is used to polish back and remove excess metal over the field regions to establish a generally flat or globally planarized surface in conjunction with an inlaid patterned metallization structure. Chemical-mechanical polishing, or CMP, increases the cost and complexity of the interconnect fabrication process.

CMP involves the application of mechanical force through pads in the presence of a suitable chemical slurry, typically applied through holes in the pad, to wear down

and selectively remove metal deposited on a substrate while the inlaid metal structures are left relatively intact due to self-aligned process end pointing. This process generates wet chemical waste that needs expensive treatment for disposal; it also requires frequent replacement of consumable pads in the CMP equipment. The CMP processes may generate and leave additional residual contaminants and particles on the wafers, thus, producing the need for post-CMP wafer cleaning.

Another difficulty with CMP is that it requires extensive equipment design and process optimization to prevent or minimize various problems such as dishing. Unless the CMP process is optimized in order to meet the process integration requirements, it can reduce the overall chip manufacturing yield and increase the chip production costs. Further, the CMP processes require relatively expensive (e.g., over $1-2 million) production equipment, resulting in additional increases in the overall semiconductor factory cost. Chemical-mechanical polishing processes are not easily integrated with copper and barrier deposition processes, resulting in increased chip manufacturing cost and production cycle time for fabrication of chips with copper wiring. For instance, the CMP-based removal rates of tantalum-based barrier materials (such as tantalum and tantalum nitride) are typically much slower than the copper removal rates, resulting in possible metal dishing problems and yield loss. Multi-step CMP processes using different chemistries may be used to alleviate this problem. Also, chemical-mechanical polishing is difficult to use with some low-k dielectrics.

A number of techniques exist for depositing a blanket layer of copper material over a substrate to fill

formations in the substrate before chemical-mechanical polishing is performed to globally planarize the substrate surface plane and remove excess copper. Metal-organic chemical-vapor deposition ("MOCVD") is a preferred deposition method for formation of seed layers for subsequent electroplating fill and for filling fine structures with large aspect ratios, such as 0.18 μm or smaller features with aspect ratios of five or greater. MOCVD advantageously deposits copper and other materials with good conformality, providing excellent gap fill qualities within small structures. However, electroplating of copper is also commonly used for larger geometry structures (e.g., $\geq$ 0.15 μm features with aspect ratios of $\leq$ 3:1).

Electroplated copper provides smooth and preferentially <111> textured films having a uniform distribution of large grains when compared with MOCVD copper films of equivalent thickness, thus providing comparable or superior electromigration characteristics. Electroplating also provides greater deposition rates when compared against MOCVD copper films, with electroplated copper typically deposited at rates grater than 4,000 Å per minute as compared to approximately $\leq$ 2,000 Å per minute for MOCVD copper.

Conventional electroplating of copper is typically performed with a copper anode and substrate wafer cathode disposed in an electrolyte bath. A current source provides current from the cathode to the anode resulting in material transferring from the anode through the electrolyte bath to the substrate wafer cathode. To achieve uniform deposition of the copper on the substrate, a seed layer (usually copper seed) is deposited on the substrate before

initiation of electroplating so that the seed layer supports current flow across the substrate surface. To deposit a continuous film of seed material, such as a copper seed film, over the surface of the substrate and within the features of the substrate, MOCVD and/or physical-vapor deposition ("PVD") such as plasma sputtering or ion-beam deposition are typically used. Generally, the seed layer should have adequate thickness to support current flow across the wafer surface, but should not have a thickness great enough to affect the characteristics of the material layer being deposited by electroplating.

One difficulty of using electroplating to deposit a material film on a substrate is that the film electroplates in a generally continuous manner across the substrate surface and within the substrate features. Thus, CMP is generally used to remove excess material following electroplating of the material. Another difficulty with electroplating copper on a substrate is that the seed layer must have adequate thickness across the substrate to conduct current in a generally uniform manner. Inadequate seed layer conductivity often results in non-uniform electroplating of material, which increases the difficulty of performing CMP with uniform end pointing. For instance, less material is generally electroplated on the substrate where current flow is restricted, such as the center of a wafer having current contact points on its periphery or outer circumference.

Another difficulty of using electroplating to deposit material on a substrate is that contact points, typically located on the frontside surface of the substrate wafer cathode to supply the current flow necessary to support electroplating, introduce additional wafer handling

difficulties and may interfere with the electroplating process preventing full-face coverage of copper. Additionally, contact points are typically located along on the periphery of the substrate, increasing the risk of non-uniform electroplating arising from diminished current flow to the center of the substrate wafer from the periphery.

SUMMARY OF THE INVENTION

Therefore, a need has arisen for a method and apparatus which electroplates a material in a substrate formation to establish a globally planarized surface.

A further need exists for a method and apparatus which electroplates a material in a substrate formation to form inlaid structures with minimal or no need for chemical-mechanical polishing of the substrate surface after deposition of the material layer.

A further need exists for a method and apparatus which electroplates material in substrate formations to form inlaid structures with minimal wafer handling complexities, wafer process time, and production waste generation.

A further need exists for a method and apparatus which enhances current distribution uniformity across a substrate surface during electroplating.

In accordance with the present invention, a method and apparatus for electroplating a material to achieve a globally planarized surface and inlaid structures is provided that substantially reduces disadvantages and problems associated with previously developed methods and apparatus for electroplating a material. Globally planarized electroplating of a material is accomplished by allowing electroplating of the material in the formations of a substrate, and suppressing electroplating of the

material at the substrate surface plane of top field regions. Globally planarized electroplating of copper material in a substrate formation enables formation of inlaid copper structures without a need for chemical-mechanical polishing or CMP.

More specifically, a membrane (preferably deformable and permeable) conforms against the substrate surface plane, suppressing the electroplating of material on the substrate surface plane. Electrolyte passes through the membrane to allow electroplating of material in formations of the substrate. Electroplating of material within the formations automatically ceases when the formations fill to the substrate surface plane and the material filling the formations comes into contact with the membrane, thus resulting in a globally planarized surface.

The membrane comprises a permeable (and electrically insulating) material that allows electrolyte to flow from the electrolyte bath into the formations of the substrate. For instance, a semi-rigid (e.g., a flexible membrane under tension), electrically-insulating polymeric membrane can be made permeable to allow electrolyte to flow to substrate formations, and strong enough to avoid rupturing if placed under mechanical stress. Nanopores formed or present in the membrane as part of the membrane structure, or alternatively by machining (e.g., micromachining) of the membrane, provide sufficient passage for electrolyte flow through the membrane. The membrane is placed proximate the substrate and conformed to the substrate surface, for instance by mechanical pressure or with hydrostatic pressure. Electrolyte between the membrane and the substrate may be periodically refreshed by removing the membrane from the substrate and then repositioning the

membrane over the substrate. Alternatively, the membrane may be rotated (or the substrate may be rotated) or otherwise moved relative to the substrate to promote flow of electrolyte to the substrate and removal of electroplating reaction byproducts. The membrane may include a conducting member for enhancing conduction of current across the surface of the substrate, enabling the usage of ultrathin seed layers.

In one embodiment a method and apparatus are provided for the introduction of current flow to support electroplating through the backside surface of the substrate. Current flows between the backside and frontside through a conducting material, such as an electrically conductive disposable dielectric and/or through the interconnects and via plugs within the substrate wafer. The backside-contacted electroplating may be accomplished with or without globally planarized electroplating provided by the membrane.

The present invention provides many important technical advantages. One important technical advantage is the electroplating of a material in device formations of a globally planarized substrate surface to form inlaid structures. The electroplating of the material in the formations to form the inlaid structures without additional electroplating of the material on the substrate field along the substrate surface plane eliminates or reduces the need for chemical-mechanical polishing. Further, the membrane advantageously ceases electroplating on a localized scale across the substrate as each structure reaches the substrate surface plane, effectively compensating for different electroplating rates in different formations comprising features with various aspect ratios. Thus, by

electroplating material on a globally planarized substrate surface and resulting in a globally planarized substrate surface, the present invention reduces chip manufacturing costs and complexity, resulting in increased yield and decreased manufacturing waste disposal problems (e.g., by eliminating the need for copper CMP process).

Another important technical advantage of the present invention is that it enhances distribution of current across the substrate to improve uniform electroplating of the material and enables reduced seed layer thickness. For instance, when electroplating is initiated, a conducting member within the membrane enhances transfer of current across the substrate surface to overcome resistance related to the use of generally thinner seed layers.

Another important technical advantage is the current flow between the backside and frontside surfaces of the substrate to support electroplating on the frontside surface. For instance, this allows more uniform electrical flow across the entire substrate surface and reduces wafer handling. Thus, the introduction of current flow through the backside surface of the substrate enhances the uniformity of current flow on the frontside surface of the substrate which in turn enhances the uniformity of electroplating material on the frontside surface of the substrate.

Another technical advantage is that when backside-contacted electroplating is used in combination with a frontside membrane, the membrane may more effectively conform to the substrate surface plane. Thus, by introducing current flow through the backside of the substrate the present invention decreases the amount of wafer handling complexity and enhances the flow of

electricity to the frontside surface of the substrate, resulting in increased electroplating effectiveness.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 depicts a side cutaway view of a substrate with inlaid metal line and via plug formations;

FIGURE 2 depicts a side cutaway view of an apparatus for electroplating material on a substrate;

FIGURE 3A depicts a top cutaway view of an apparatus for electroplating material on a substrate;

FIGURE 3B depicts a top view of a membrane and conducting member;

FIGURE 4A depicts a side cutaway view of a membrane conformed against the field region of a substrate along the substrate surface plane; and

FIGURE 4B depicts a side cutaway view of a device formed by globally planarized electroplating.

FIGUREs 5 and 5A depict a side cutaway view of an apparatus for electroplating material on a substrate by flowing current between the backside and frontside of the substrate.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the present invention are illustrated in the figures, like numeral being used to refer to like and corresponding parts of the various drawings.

Damascene techniques for copper deposition support the fabrication of inlaid copper interconnect lines and plugs within substrate formations. However, the reliance of damascene techniques on chemical-mechanical polishing to form the inlaid metallization structures and establish a globally planarized substrate surface plane presents a number of disadvantages. The present invention advantageously supports fabrication of high performance inlaid interconnect structures, such as copper metallization, by depositing material in substrate formations along a globally planarized substrate field surface. Globally planarized electroplating of a material in substrate formations without electroplating material on the field regions of the substrate plane eliminates or substantially reduces the need for chemical-mechanical polishing by suppressing electroplating of material on or above the substrate surface plane. Although described herein as forming inlaid copper interconnects, the present invention will also support electroplating of other interconnect metallization materials and will support deposition in conjunction with conventional dielectric materials, low-k dielectric materials, and free-space interconnect dielectrics.

Referring now to FIGURE 1, some of the difficulties associated with obtaining a globally planarized substrate surface plane using chemical-mechanical polishing are apparent. A side cutaway view of a device or interconnect structure 10 depicts a substrate 12, such as a silicon substrate, having a diffusion barrier layer 14 and a copper layer 16 deposited upon it. Formations or patterned features established in device 10 include trenches for inlaid lines 18 and holes for inlaid plugs 20 formed within

inter-metal/inter-level dielectric medium 15 in substrate 12. Copper layer 16 has been deposited to form inlaid metal lines 18 and inlaid via plugs 20 within dielectric metal trenches and via holes, but has also been deposited above the initial substrate surface plane 22. Known chemical-mechanical polishing (CMP) techniques can preferentially remove copper layer 16 starting from the topmost regions down to substrate surface field plane 22 to complete formation of inlaid metal lines 18 and inlaid via plugs 20, without any substantial removal of the inlaid copper lines and plugs below the surface plane 22.

The present invention provides for uniform void-free material electroplating within substrate formations or inlaid trenches and holes, and also suppresses or eliminates material deposition above the substrate surface plane along the substrate field to achieve fabrication of inlaid metallization or wiring structures with a globally planarized surface without a need for a CMP fabrication process. Referring now to FIGURE 2, a side cutaway view of an apparatus for globally planarized electroplating is depicted. A stretched membrane 32 suppresses electroplating of material on substrate wafer 12 surface, but allows electrolyte to pass through the membrane to electroplate material in the formations of substrate 12.

Electroplating apparatus 30 uses a voltage or current source 34 to electroplate material from an anode 36 to a substrate 12, which acts as the cathode of the electroplating circuit. Electrolyte inlets 38 provide fresh electrolyte to support transfer of charged materials from anode 36 to substrate 12 through an electrolyte bath 46. Used electrolyte exits apparatus 30 through electrolyte outlets 40. A distributor plate 42 disposed

between anode 36 and substrate 12 helps to maintain uniform electrolyte flow across substrate 12. A housing 44 contains the electrolyte bath 46, and may electrically isolate anode 36 and wafer cathode 12 or may act as the ground for current source 34. An anode support 48 and substrate support 50 align anode 36 and a substrate 12 acting as a cathode in a generally parallel configuration within electrolyte bath 46.

As with conventional electroplating, apparatus 30 may electroplate copper from a copper anode 36 to formations in substrate 12 through electrolyte bath 46 using current source 34. Charged copper from anode 36 is distributed in a generally uniform manner across substrate 12 to electroplate on the exposed surface of substrate 12. Membrane supports 52 hold membrane 32 proximate to substrate 12 so that electrolyte carrying copper from anode 36 must pass through membrane 32 to reach the surface of substrate 12. Membrane supports 52 and membrane 32 are electrically non-conducting materials that are electrically isolated from substrate 12 to minimize electroplating of copper on membrane 32. The membrane itself is preferably made of an electrically insulating material to prevent interference with the electroplating process.

In one embodiment, membrane supports 52 may move membrane 32 relative to substrate 12 to enhance the flow of electrolyte from electrolyte bath 46 to substrate 12. For instance, membrane supports 52 or substrate supports 50 may rotate so that relative movement exists between membrane 32 and substrate 12. Alternatively, membrane supports 52 may mechanically remove membrane 32 from substrate 12 periodically to allow fresh electrolyte to flow between membrane 32 and substrate 12. Membrane supports 52 may

then replace membrane 32 proximate to and in contact to substrate 12 creating a mechanical contact force that presses membrane 32 against substrate 12. To further conform membrane 32 against substrate 12, hydrostatic pressure of electrolyte flow from electrolyte inlet 38 may be used to force membrane 32 against substrate 12. To minimize inadvertent electroplating of material on field regions of substrate 12, current source 34 may be turned off or reversed in polarity while membrane 32 is away from substrate 12, and then turned back on with the desired deposition-mode polarity when membrane 32 is returned to contact to substrate 12. In other words, power may be time modulated with the position of the membrane so that power is turned off when the membrane is distal the substrate, allowing fresh electrolyte proximate the field surface without material being deposited on the surface.

Referring now to FIGURE 3A, a top cutaway view of electrolyte apparatus 30 is depicted. Substrate 12 and anode 36 generally have a circular geometry with approximately the same diameters. Membrane 32 also has a circular geometry with a diameter slightly larger than substrate 12 so that the stretched membrane 32 may cover the entire exposed surface of substrate 12 conformally during electroplating. Distributor plate 42 has plural distribution holes to distribute the flow of electrolyte through housing 44. In alternative embodiments, different shaped and sized substrates, anodes and membranes may be used so long as membrane 32 is disposed proximate to and preferably in contact to substrate 12 and between substrate 12 and anode 36 for those areas of the field of substrate 12 in which electroplating of material from anode 36 is to be suppressed or prevented.

Referring now to FIGURE 3B a top view of a membrane 32 having an inlaid conducting member 54 is depicted. One difficulty associated with suppressing the electroplating of material on a substrate surface while also electroplating material in formations of the substrate is that a uniformly electroplated layer will not be created to help support uniform current flow across a substrate 12. For instance, current from current source 34 is typically conducted to substrate 12 by contact pins in physical contact with the outer circumference of substrate 12. If electroplating is suppressed on the field region of substrate 12 by contact with membrane 32 along the substrate surface plane 22, then the resistance to current flow across substrate 12 depends on the sheet resistance of the initial seed layer over the substrate and the thickness of the layer electroplated across the surface of substrate 12. Conducting member 54 is an electrically conducting material embedded in membrane 32 (resulting in a planarized surface) to promote uniform conduction of current across substrate 12 from edge towards center. The spiral shape of conducting member 54 contacts the surface of substrate 12 for promoting uniformity of electric current flow across the surface. In alternative embodiments, other geometries may be used for embedded conducting member 54 to promote uniform current flow. The membrane and the substrate may have relative rotation with respect to each other to enable uniform formation of the inlaid lines and plugs.

Referring now to FIGURE 4A, a side cutaway view of a membrane 32 conformed to the surface plane of 22 of substrate 12 is depicted. Membrane 32 is a semirigid, electrically insulating permeable material, such as a polymeric material or a micromachined inorganic membrane,

that conforms along substrate surface plane 22 but leaves a cavity where substrate formations, such as wire line trenches 18 and via plug holes 20, have been patterned into substrate 12. The proximity of membrane 32 with substrate 12 suppresses the electroplating of copper along the field regions associated with the substrate surface plane 22. However, electrolyte flows with charged copper particles from electrolyte bath 46 through nanopores 56 formed in membrane 32 to support electroplating of copper in the formations 18 and 20 of substrate 12. Nanopores 56 may be machined (e.g., by chemical etch or plasma etch micromachining) in membrane 32 or may be formed as part of the structure of the material of membrane 32. The membrane may be cleaned periodically by applying a reverse polarity to the electroplating apparatus.

To initiate electroplating of copper, a pattern substrate 12 has a barrier 14 laid on it that prevents diffusion of copper into substrate 12. A seed layer 58 is then deposited on top of barrier layer 14. Seed layer 58 provides sufficient electrical conductivity across surface plane 22 of substrate 12 to support uniform current flow. For instance, seed layer 58 may be a 100 to 500 Å thick layer of copper. Seed layer 58 and barrier 14 may be deposited with conventional chemical-vapor deposition, physical-vapor deposition, ion-beam deposition, or other thin-film deposition methods.

Once substrate 12 has a seed layer of adequate thickness to support electrical conduction across substrate surface plane 22, membrane 32 is pressed against substrate surface plane 22 to conform against the field region along entire substrate surface plane 22. The proximity of membrane 32 with substrate 12 suppresses electroplating of

copper on top of seed layer 58 except for electroplating that occurs within formations 18 and 20. Electroplating in the formations automatically ceases as the formations fill with copper material so that the structures electroplated in the formations touch membrane 32. Complete filling of the formation may be detected in real time by a suitable end pointing method such as an electrical end pointing method. Once the formations are filled with material, the membrane is removed or separated from the substrate, leaving a globally planarized surface along substrate surface plane 22, with copper structures fabricated in formations 18 and 20 of substrate 12 and barrier 14 and seed layer 58 remaining over the field of substrate 12.

Referring now to FIGURE 4B, a device 10 is depicted with copper deposited in wire line 18 and via plug 20 of substrate 12. Seed layer 58 and barrier 14 deposited along substrate surface plane 22 have been removed (e.g., by ion-beam etching) to expose field regions of substrate 12. Seed layer 58 and barrier 14 may be removed with, for instance, reactive ion etch or ion-beam etching or with etch performed by simply reversing the voltage of current source 34 in the electrochemical deposition bath. Copper electroplated in formations 18 and 20 automatically ceases its growth when it comes into contact with membrane 32. One advantage of the automatic ceasing of electroplating is that the formations 18 and 20 will uniformly fill to substrate surface plane 22 even when electroplating rates are uneven across substrate 12.

Referring now to FIGUREs 5 and 5A, a side cutaway view of an apparatus for electroplating material onto a substrate is depicted. Current source 34 interfaces with the substrate wafer 12 through a cathode contact 66 at one

or more cathode contact points 67 located on the backside surface 68 of the substrate wafer 12. Current from the current source 34 flows between substrate 12, which acts as the cathode of the electroplating apparatus, and anode 36, which provides the material to be electroplated. Contact region 67 interfaces with current source to pass current between the backside 68 of wafer 12 and the frontside 70. Current may pass through the array of devices, interconnects and via plugs 72 within the substrate to provide a current flow path between frontside surface 70 and backside surface 68 of the substrate 12. In one embodiment, the cathode contact 66 or contact region 67 comprise a resistor associated with the backside surface 68 to regulate current flow.

In an alternative embodiment the inter-level/inter-metal dielectric layers of substrate 12 are comprised of a disposable electrically conductive material that supports current flow between the frontside and backside of substrate 12. For instance, U.S. Patent Application Serial No. 09/064,431, entitled "Ultra High-Speed Chip Interconnect Using Free Space Dielectrics," by Moslehi, assigned to CVC Products, Inc. and incorporated herein by reference, discloses a disposable dielectric that is removed during device fabrication to leave a free-space dielectric. If the disposable dielectric is a conductive material, such as of silicon and a conductive dopant, then the disposable dielectric supports current flow from the backside to the frontside of substrate 12. The disposable conductive layer allows current to flow from one or more cathode contacts 66 disposed across the backside 68 of substrate 12 to evenly spread the current flow, and then flow through the disposable conductive layer to the

frontside surface plane 70. A membrane for establishing a globally planar electroplated surface may also be associated with frontside surface 70 as discussed above. After electroplating is complete the conductive disposable layer may be removed leaving a free-space dielectric in the space which had contained the disposable layer. According to this embodiment the need for a seed layer is reduced or eliminated.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made thereto without departing from the sphere and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method for depositing a material on a substrate, the method comprising the steps of:

conforming a membrane against the substrate surface plane so that the membrane contacts the surface field of the substrate; and

passing electrolyte through the membrane, the electrolyte electroplating the material in the formations of the substrate.

2. The method of Claim 1 wherein the material comprises copper, the method further comprising the step of providing an electrical current for transferring copper from a copper anode through the electrolyte and through said membrane to the substrate.

3. The method of Claim 2 further comprising the step of refreshing the electrolyte within the formations.

4. The method of Claim 3 wherein said refreshing step comprises moving the membrane relative to the substrate.

5. The method of Claim 4 wherein said movement comprises rotation of said membrane relative to the substrate.

6. The method of Claim 3 wherein said refreshing step comprises periodic engagement and disengagement of said membrane relative to said substrate in conjunction with changing the electroplating current between the membrane engagement and disengagement periods.

7. The method of Claim 3 wherein said refreshing step further comprises the steps of:

removing the electrical current;

removing the membrane from the substrate surface plane so that fresh electrolyte flows between the membrane and the substrate;

re-conforming the membrane against the substrate surface plane; and

re-applying the electrical current for transferring copper from the copper anode through the electrolyte to the substrate.

8. The method of Claim 1 wherein the membrane comprises a permeable, electrically-insulating material.

9. The method of Claim 1 wherein the membrane comprises a polymeric material.

10. The method of Claim 1 wherein the membrane is a micromachined plate.

11. The method of Claim 9 wherein the membrane further comprises an electrically-conducting member distributed throughout the membrane to promote electrical conduction across the substrate upon contact between the membrane and the substrate.

12. The method of Claim 1 further comprising the step of conducting current through the membrane to improve the electrical conductance between the center portion and outer portion of the substrate during electroplating.

13. The method of Claim 1 wherein said conforming step further comprises asserting hydrostatic pressure to conform the membrane to the substrate surface plane.

14. The method of Claim 13 wherein said hydrostatic pressure is applied through the electrolyte medium, promoting electrolyte flow through the membrane to the substrate formations.

15. A method for globally planarized electroplating of a material on a substrate, the method comprising the steps of:

electroplating the material from an anode to the substrate, the material filling a formation of the substrate;

suppressing the electroplating of the material on the field surface of the substrate; and

ceasing the electroplating of the material when the material fills the formation.

16. The method of Claim 15 wherein said suppressing step comprises placing a membrane in contact with the field surface of the substrate.

17. The method of Claim 16 wherein said placing step comprises applying hydrostatic pressure through the electrolyte to the membrane so that the membrane conforms to the field of the substrate across the entire substrate surface plane.

18. The method of Claim 15 wherein the material comprises copper.

19. The method of Claim 18 further comprising the step of removing copper deposited on the field of the substrate.

20. The method of Claim 19 wherein said removing step comprises performing an in-situ etch to remove copper from the field of the substrate.

21. The method of Claim 19 wherein said removing step comprises performing plasma or ion-beam etch to remove copper and any underlying barrier from the field of the substrate.

22. The method of Claim 16 wherein said ceasing step comprises automatically suppressing the electroplating of material in the formation when the material growth brings the material into contact with the membrane.

23. The method of Claim 22 wherein said ceasing step utilizes an electrical end pointing step.

24. An apparatus for electroplating a material onto a substrate, the substrate having a field and formations, the apparatus comprising:

a housing operational to hold an electrolyte bath;

an anode support disposed in the housing;

a substrate support disposed in the housing;

a current source interfaced with the anode support and the substrate, the current source operational to support electroplating from an anode associated with the anode support through the electrolyte to a substrate associated with the substrate support;

a membrane disposed in the housing, the membrane operational to pass electrolyte to the formations of the substrate for electroplating the material in the formations, the membrane further operational to suppress electroplating of the material on the field surface of the substrate.

25. The apparatus of Claim 24 wherein the material comprises copper.

26. The apparatus of Claim 24 further comprising an edge ring disposed proximate the substrate, the edge ring operational to support the membrane in contact with the field of the substrate.

27. The apparatus of Claim 26 further comprising electrolyte supplied to the housing such that the electrolyte provides hydrostatic pressure to conform the membrane to the substrate field surface.

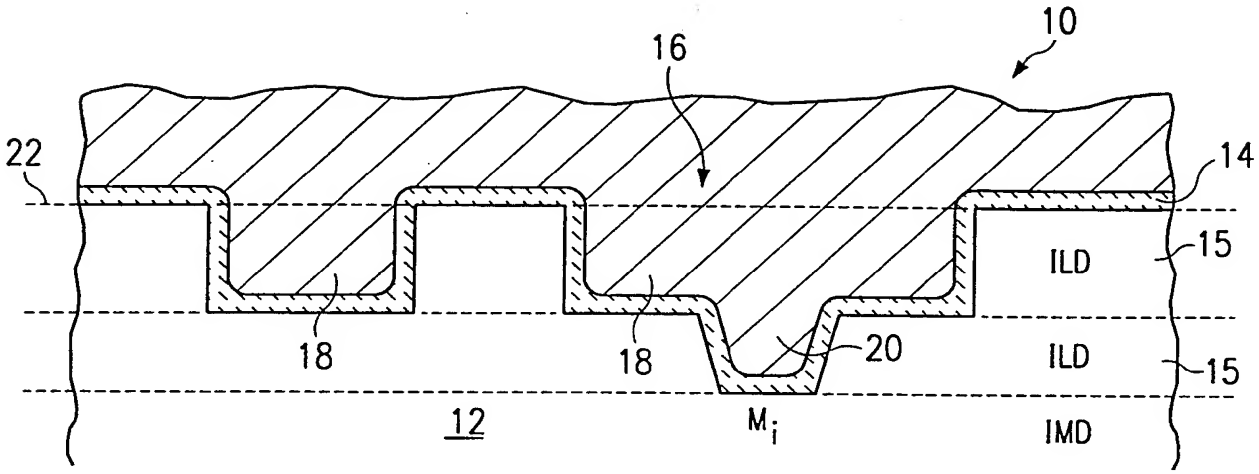


FIG. 1

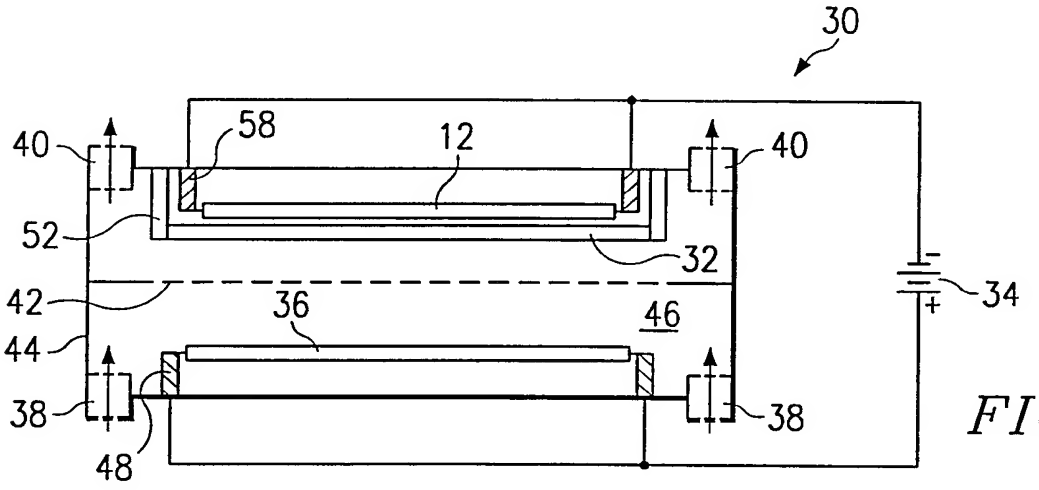


FIG. 2

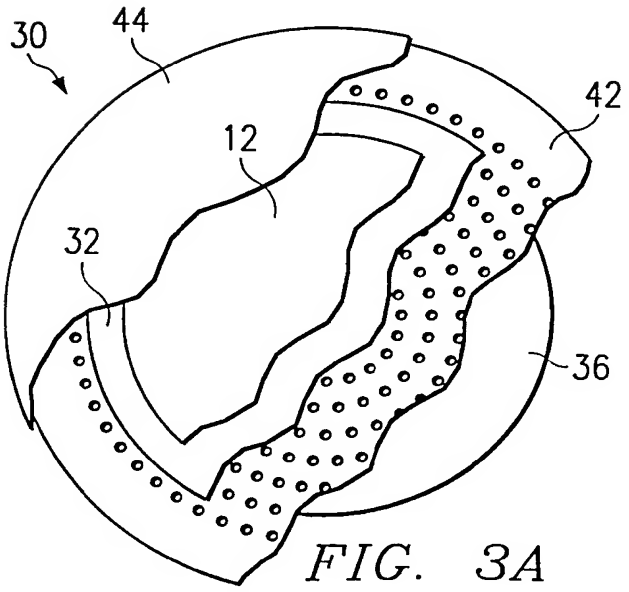


FIG. 3A

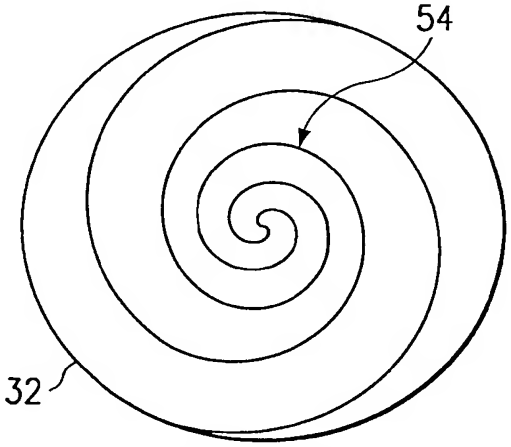
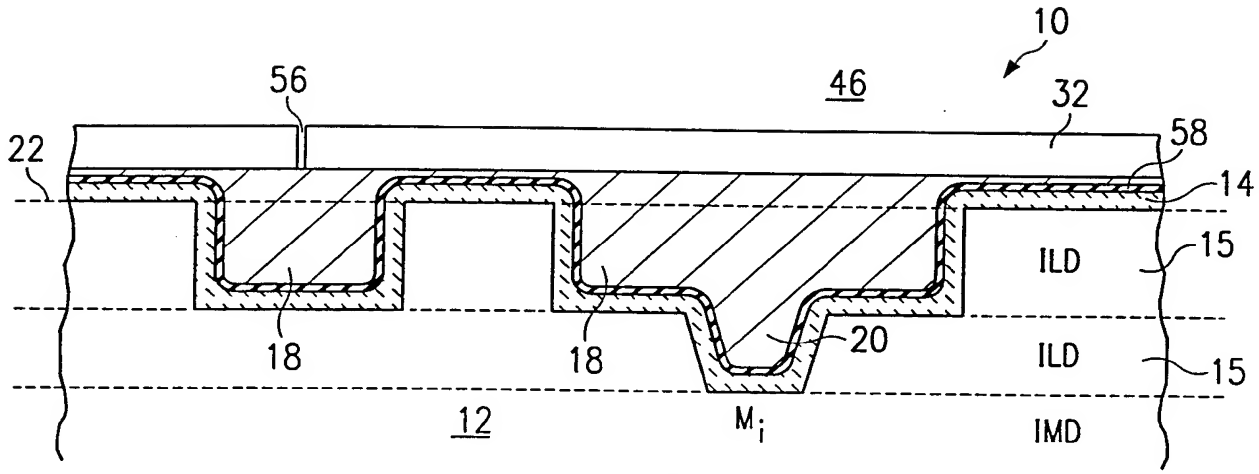


FIG. 3B


10
56
46
32
58
22
14
ILD
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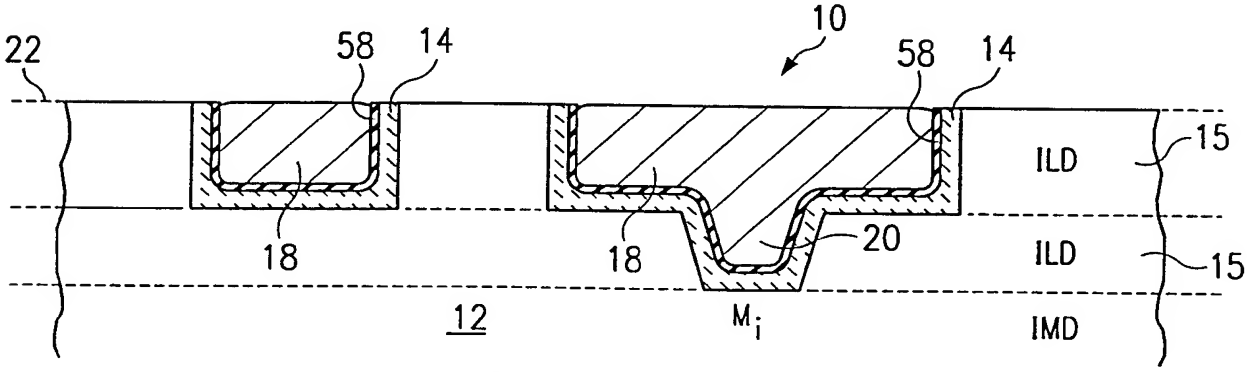
18
18
20
ILD
15
12
M_i
IMD

FIG. 4A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ILD
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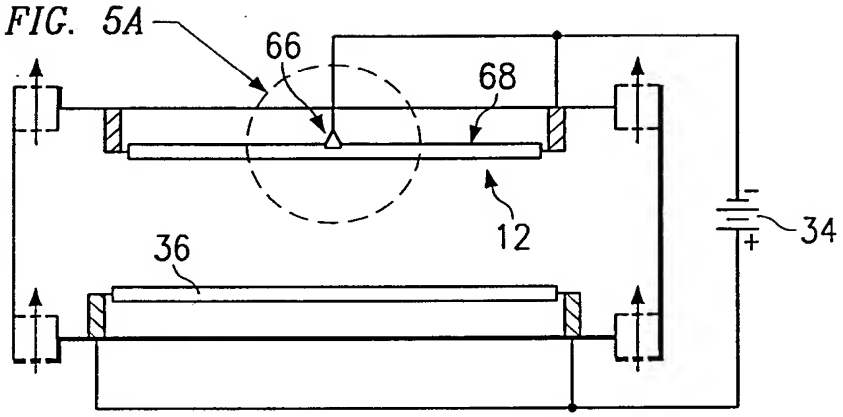
ILD
15
12
M_i
IMD

FIG. 4B

FIG. 5



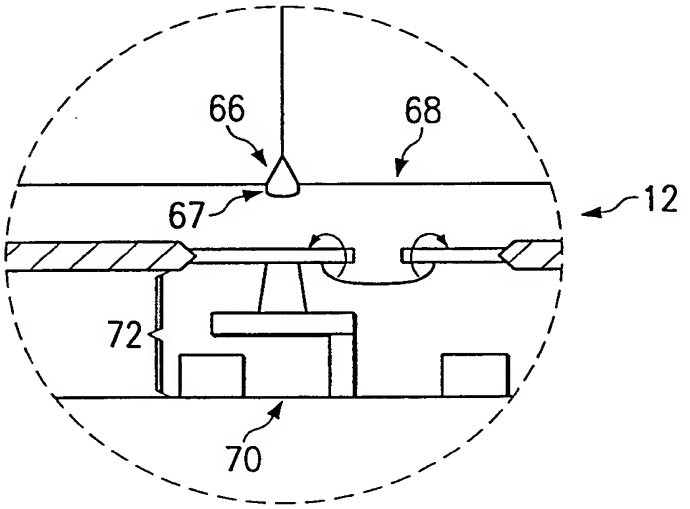


FIG. 5A

INTERNATIONAL SEARCH REPORT

Int. ational Application No
PCT/US 00/16078

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 C25D5/02 C25D7/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 C25D H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 00 26443 A (NUTOOL INC) 11 May 2000 (2000-05-11) page 2, line 6 - line 30 page 3, line 17,18 page 3, line 27 - line 31 page 4, line 27 -page 5, line 2 page 5, line 13 - line 25 page 5, line 27 - line 29 page 6, paragraphs 1,4 claims figures --- -/--	1-5,8,9, 15,16, 18-20, 22,24,25

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 October 2000	02/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Zech, N

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Im. .ational Application No
PCT/US 00/16078

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